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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/407,204	09/28/1999	MING-TUNG SHEN	8688.128US01	2434

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/407,204	Shen
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Nov 25, 2002*.

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1, 3-6, and 19-21* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 3-6, and 19-21* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☒ Interview Summary (PTO-413) Paper No(s). 16
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Objections

1. Claims 3, 5 and 6 are objected to because of the following informalities: .

Claims 3, 5, and 6, line 1: Delete ...."claim 2...." and insert ----"claim 1"----.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-6 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al (US Pat. 6051878) in view of Bertin et al (US Pat. 5977640) and Panchou et al (US Pat. 6040630).

Regarding claim 1, Akram et al disclose a semiconductor stacked device/multichip module(MCM) comprising:

- a chip mounting member/printed circuit board-PCB (140 in Fig. 1; Col. 4, line 50) having opposite first and second surfaces (146/142 in Fig. 1), conventional bond pads and a set of first circuit traces on each surface (Col. 4, line 30) and a plurality of through holes/vias (158 in Fig. 1) that extend in/on the first and second surfaces and are connected to the circuit traces (see through holes/vias 158/136 extending through the substrates 140/116; Col. 6, line 25-55; Col. 10, line 10-20)
- a first semiconductor chip (162 in Fig. 1) on the top surface of the PCB, the chip having a pad mounting surface with a plurality of flip chip contact pads (not numerically referenced in Fig. 1; Col. 4, line 10; Col. 6, line 55) provided thereon
- a first conductor units/contacts including a plurality of conventional flip chip bumps (166 in Fig. 1) for electrically connecting the contact pads of the semiconductor chips and the first circuit traces
- the first traces and the chip being disposed on the same surface (146 in Fig. 1) of the chip mounting member
- a first conventional flip chip dielectric material/adhesive member (168 in Fig. 1) for bonding adhesively the first chip on the chip mounting member, and
- a plurality of conventional external connections comprising solder balls, columns, etc. (148 in Fig. 1; Col. 3, line 55) disposed on one or both surfaces of the chip mounting

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- a first conductor units/contacts including a plurality of conventional flip chip bumps (166 in Fig. 1) for electrically connecting the contact pads of the semiconductor chips and the first circuit traces
- the first traces and the chip being disposed on the same surface (146 in Fig. 1) of the chip mounting member
- a first conventional flip chip dielectric material/adhesive member (168 in Fig. 1) for bonding adhesively the first chip on the chip mounting member, and
- a plurality of conventional external connections comprising solder balls, columns, etc. (148 in Fig. 1; Col. 3, line 55) disposed on one or both surfaces of the chip mounting

member, the solder balls/columns being aligned with and connected to the respective bond pads and through holes/vias in the chip mounting member (see through holes/vias 136 through the substrate 116 in Fig. 1; Col. 6, line 40; Col. 4, line 20-57) (Fig. 1; Fig. 1-6; Col. 3-10).

Akram et al further disclose the through holes/vias and traces electrically connecting the top and bottom surfaces of the chip mounting substrates (136, 156, etc. in Fig. 1; Col. 6) but Akram et al fail to specify:

a) the through holes being plated through holes, and

b) using a first dielectric tape member as an adhesive member, the tape being formed with the a plurality of holes at positions registered with the contacts/pads of the chip and a first conductor unit including a plurality contact balls that are received in the holes of the tape to establish the electrical connection between the chip and the first circuit traces.

a) Bertin et al teach using a wiring in a variety of configurations such as conductive traces, through-holes/channels comprising plated solder, copper, etc. (25 in Fig. 3, 7, 16, etc., Col. 3, line 5-10) to provide an electrical connection through/within the substrate with respectively aligned solder balls.

b) Panchou et al teach using an attachment film/dielectric tape with a plurality of holes (30/34 in Fig. 4a) at positions in registration with the corresponding contact pads of a chip (12 in Fig. 4a). Panchou et al further teach having a first conductor unit/structure comprising pads and contact bumps/balls (12 and 14 respectively in Fig. 4a) being positioned/received in the respective holes to provide an adhesive bonding and an electrical interconnection for a flip chip device (Fig. 4/4a; Col. 4 and 5).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate plated through holes as taught by Bertin et al and a first dielectric tape member as an adhesive member, the tape being formed with the a plurality of holes at positions registered with the contact pads of the chip and a first conductor unit including a plurality contact balls that are received in the holes of the tape to establish the electrical connection between the chip and the first circuit traces as taught by Panchou et al so that the substrate/chip bonding strength and interconnection reliability can be improved in Akram et al's chip module.

Regarding claim 3, as explained above for claim 1, Akram et al further disclose the module having a plurality of chips and substrates/mounting members including a first and second chip, the module further comprising:

- a set of second circuit traces accessible from the second surface of the chip mounting member (154 in Fig. 1) and connected to the through holes/vias (158 in Fig. 1), that

extend within and on the first and second surfaces and are connected to the circuit traces (Col. 6, line 50), and

- a second semiconductor chip having a pad mounting surface (152 in Fig. 1) and a plurality of conventional contact pads being in electrical communication with the circuit traces on the surface (not numerically referenced in Fig. 1; Col. 4, line 30), the chip being bonded by conventional wire bonding, flip chip bonding using an adhesive, conductive adhesive, etc. (Col. 4, line 10-15; Col. 6; Fig. 1 and 4-6).

Regarding claim 4, Akram et al fail to specify using a second dielectric tape adhesively bonding the second chip, the tape having a plurality of holes at positions being in registration with the corresponding contact pads and the holes receiving the plurality of contact balls to provide an electrical connection between the second chip to the second circuit traces.

As explained above for claims 1 and 3, Panchou et al teach using an attachment film/dielectric tape with a plurality of holes (30/34 in Fig. 4a) at positions in registration with the corresponding contact pads of a chip (12 in Fig. 4a). Panchou et al further teach having a first conductor unit/structure comprising pads and contact bumps/balls (12 and 14 respectively in Fig. 4a) being positioned/received in the respective holes to provide an adhesive bonding and an electrical interconnection for a flip chip device (Fig. 4/4a; Col. 4 and 5).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate plated through holes as taught by Bertin et al and a second dielectric tape having a plurality of holes at positions being in registration with the corresponding contact pads and the holes receiving the plurality of contact balls to provide an adhesive bonding and an electrical connection between the second chip to the second circuit traces as taught by Panchou et al so that the substrate/chip bonding strength and interconnection reliability can be improved in Akram et al's multichip chip module.

Regarding claim 5, Akram et al further disclose providing a conventional polymer resin/epoxy (168 in Fig. 1; Col. 6, line 60) on a peripheral portion of the chip and the same (168/170 in Fig. 1; Col. 6, line 60-65) on the surfaces of the chip mounting member/PCB to strengthen the bonding of the first semiconductor chip and to provide added protection for the module.

Regarding claim 6, Akram et al fail to specify securing a heat dissipating plate on the heat dissipating surface opposite to the pad mounting surface of the chip.

Bertin et al teach using conventional heat spreader/plate secured on the heat dissipating surface opposite to the pad mounting surface of the chip (Fig. 7 and 15; Col. 4, line 16) to improve heat dissipation.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a heat dissipating plate on the heat dissipating surface opposite to the pad mounting surface of the chip as taught by Bertin et al so that heat dissipation can be improved in Akram et al's module.

Regarding claim 19, as explained above for claims 1, 3 and 4, Akram et al further disclose using a variety of configurations comprising a stacking of two or more semiconductor chip modules having an upper and lower module, the modules being aligned with respective external pin, solder ball or column connections with corresponding traces/through-holes to form a multiple stack (Fig. 1; Col. 3, line 55; Col. 4, line 20-57; Col. 6, line 40).

Regarding claim 20, as explained above for claims 1, 3, 4 and 19, Akram et al fail to specify:

a) the through holes being plated through holes, and

b) using a first and second dielectric tape member as an adhesive member, each tape being formed with the a plurality of holes at positions registered with the contacts/pads

of the chip and a first and second conductor unit including a plurality contact balls respectively that are received in the holes of the tape to establish the electrical connection between the first and second chip and respective first and second circuit traces.

a) Bertin et al teach using a wiring in a variety of configurations such as conductive traces, through-holes/channels comprising plated solder, copper, etc. (25 in Fig. 3, 7, 16, etc., Col. 3, line 5-10) to provide an electrical connection through/within the substrate with respectively aligned solder balls.

b) Panchou et al teach using an attachment film/dielectric tape with a plurality of holes (30/34 in Fig. 4a) at positions in registration with the corresponding contact pads of a chip (12 in Fig. 4a). Panchou et al further teach having a first conductor unit/structure comprising pads and contact bumps/balls (12 and 14 respectively in Fig. 4a) being positioned/received in the respective holes to provide an adhesive bonding and an electrical interconnection for a flip chip device (Fig. 4/4a; Col. 4 and 5).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate plated through holes as taught by Bertin et al and a first and second dielectric tape having a plurality of holes at positions being in registration with the corresponding contact pads and the holes receiving the plurality of contact balls to provide an adhesive bonding and an electrical connection between the

first and second chip to respective first and second circuit traces as taught by Panchou et al so that the substrate/chip bonding strength and interconnection reliability can be improved in Akram et al's multichip chip module.

Regarding claim 21, as explained above for claims 1, 19 and 20, Akram et al further al teach using each of the solder balls being connected to one of the first and second circuit traces.

Response to Arguments

3. Applicant's arguments filed on 11-25-02 have been fully considered but they are not persuasive.

A. Applicant contends that Panchou et al disclose a tape member but do not disclose a conductor unit having contact balls being received in the holes of the tape.

However, as explained above, Panchou et al teach using a conventional attachment film/dielectric tape having a plurality of holes (34 in Fig. 4) and a conductor unit structure where the holes in the tape are positioned/formed to receive the conductors such as contact bumps/balls (14 in Fig. 4a) for the flip chip device.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

NP
01-31-03

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